UNITED STATES PATENT APPLICATION

for

A LVDS OUTPUT DRIVER HAVING LOW SUPPLY VOLTAGE CAPABILITY

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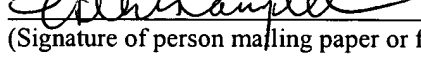
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REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of U.S. Provisional Application No. 60/463,827, filed on April 17, 2003.

FIELD OF INVENTION

[0002] The present invention relates generally to integrated circuit output drivers, and more particularly, to low voltage differential signal (LVDS) output drivers.

BACKGROUND

[0003] Low-Voltage Differential Signaling (LVDS) is an interface standard that can be used for high-speed data transmission. By using low swing signals (typically about 300mV), fast bit rates, lower power, and better noise performance can be achieved. The differential nature allows for increased noise immunity and noise margins. Examples of applications that use LVDS signaling include hubs for data communications, base stations and switches for telecommunications, flat-panel displays and servers, peripheral devices including printers and digital copy machines, and high-resolution displays for industrial applications.

[0004] Most integrated circuit (IC) or "chip" driver circuits designed to implement an LVDS interface include circuits that use a 2.5V or higher power supply. A typical conventional driver circuit design is shown in Figure 1. The circuit includes two operational amplifiers (amp1 and amp2) to generate internal vdd_voh and vss_vol power supplies, respectively. The p-type metal oxide semiconductor (PMOS) (i.e., p-channel) and n-type metal oxide semiconductor (NMOS) (i.e., n-channel) transistors referenced to these supplies can be designed to produce the desired signal swing and common mode

voltage. These switching transistors connected to vdd_voh and vss_vol require full rail (about 2.5V in this example) complementary metal oxide semiconductor (CMOS) signal levels at their gates to fully switch the output transistors (e.g., Q5, Q6, Q7 and Q8). The skew between input true and complement signals are very low to achieve the signal integrity specified in the LVDS standard. For clarity, the low voltage to high voltage level translators as well as additional conventional circuitry to minimize the skew are not shown in Figure 1.

[0005] Disadvantages of the above approach include a lack of functionality at lower power supplies, such as about 1.8V or lower, using transistors with a 2.5V compatible process. According to one LVDS standard, the nominal output common mode voltage is about 1.25 volts. This further requires a sufficient drive on the NMOS output transistors (Q6 and Q8) to accommodate the Vol (maximum output voltage for "low" signal detection) specification. In the above design, the NMOS output transistors (Q6 and Q8), for example, will not sufficiently turn on at such low voltage to provide the appropriate output levels and signal integrity over process/voltage/temperature (PVT) corners with a power supply at or below approximately 1.8V.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention will be understood more fully from the detailed description that follows and from the accompanying drawings, which however, should not be taken to limit the appended claims to the specific embodiments shown, but are for explanation and understanding only.

[0007] Figure 1 shows an existing LVDS output driver.

[0008] Figure 2 shows one embodiment of a LVDS output driver having low supply voltage capability.

[0009] Figure 3 shows one embodiment of a process to output low voltage differential signals.

[0010] Figure 4 shows one embodiment of a process to generate differential low swing signals using a low swing differential pre-driver.

[0011] Figure 5 shows an exemplary embodiment of a networked system.

DETAILED DESCRIPTION

[0012] In the following description, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known circuits, structures, and techniques have not been shown in detail in order not to obscure the understanding of this description.

[0013] Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification do not necessarily all refer to the same embodiment.

[0014] Figure 2 shows one embodiment of a LVDS output driver having low supply voltage capability in an electronic device. The LVDS output driver 200 includes a pair of pull-up transistors Q11 and Q12, a pair of pull-down transistors Q13 and Q14, a pair of NMOS transistors Q15 and Q16, a first pair of inverters 251 and 252, a first current source Q19, a pair of PMOS transistors Q17 and Q18, an operational amplifier 230, a second current source Q9, a second pair of inverters 241 and 242, a current sink 245, and a load R1.

[0015] In one embodiment, each of the pull-down transistors Q13 and Q14 are each configured as a source follower. Each of the pull-down transistors Q13 and Q14 includes a source, a drain, a gate, and a bulk terminal. In one embodiment, the pull-down transistors Q13 and Q14 are PMOS transistors. The source of each of the pull-down

transistors Q13 and Q14 may be coupled to the bulk terminal of the corresponding pull-down transistor to reduce the body effect on the corresponding pull-down transistor.

[0016] Two differential input signals, cmos_in_p 201 and cmos_in_n 202, are input to the LVDS output driver 200. The differential input signals may come from the core logic (not shown) of the electronic device. In one embodiment, the inverters 251 and 252 amplify the differential input signals 201 and 202, respectively. Then the inverters 251 and 252 may output the amplified input signals to the pull-up transistors Q11 and Q12. The inverters 251 and 252 may be powered by the voltage vdd_low 206. In some embodiments, vdd_low 206 is approximately between 1.1V and 1.3V. In one embodiment, the pull-up transistors Q11 and Q12 are PMOS transistors, each having a gate, a source, and a drain. The amplified input signals may be applied to the gates of the PMOS transistors Q11 and Q12. Furthermore, the drains of the PMOS transistors Q11 and Q12 may each be coupled to the sources of the pull-down transistors Q13 and Q14, respectively, to output the low voltage differential signals, lvds_out_p and lvds_out_n, respectively. In one embodiment, the PMOS transistors Q13 and Q14 are, respectively, biased by the NMOS transistors Q15 and Q16, which are coupled to each other at the gates of the NMOS transistors Q15 and Q16. A biasing voltage, oss_bias 207 may be applied to the gates of the NMOS transistors Q15 and Q16.

[0017] Unlike the existing design, the pull-down transistors Q13 and Q14 are driven by a pair of low swing differential signals. In one embodiment, the low swing differential signals are generated by a low swing differential pre-driver 240. The low swing differential pre-driver 240 may include the inverters 241 and 242, the load R1, the current source Q9, and the current sink 245. The inverters 241 and 242 may amplify the

input differential signals 201 and 202, respectively, and output each of the amplified signals to each one of the nodes 281 and 282 of the load R1. The load R1 may include a resistor. The current source Q9 supplies a current to the load R1, which drains the current via the current sink 245. The current source Q9 may include a PMOS transistor powered by vdd_low 206. In some embodiments, vdd_low 206 is approximately between 1.1V and 1.3V. The current sink 245 may include an NMOS transistor Q10 and a resistor R2 coupled to each other in parallel. The NMOS transistor Q10 may be driven by a biasing voltage, nbias 285. The PMOS transistor Q9 may be driven by a biasing voltage, pbias 286. The low swing differential pre-driver 240 outputs the low swing differential signals dfl_p and dfl_n at the nodes 281 and 282, respectively. The low swing differential signals dfl_p and dfl_n may be applied onto the gates of the pull-down transistors Q14 and Q13, respectively, to drive the pull-down transistors.

[0018] In one embodiment, the sources of the pull-up transistors Q11 and Q12 are coupled to the current source Q19. The current source Q19 may include a PMOS transistor powered by vdd_io 203. In one embodiment, the range of vdd_io 203 is about 1.624 volts to 2.725 volts. The gate of the PMOS transistor of the current source Q19 may be coupled to an output of the operational amplifier 230, which drives the current source Q19 in response to an input signal to the operational amplifier 230, voh_ref 205 and voh_sense 208.

[0019] Furthermore, the drain of the PMOS transistor of the current source Q19 may be coupled to a sensing circuit 235. The sensing circuit senses the higher output voltage among the output voltages, lvds out_p 291 and lvds out_n 292, to generate the feedback signal, voh_sense 208. The sensing circuit 235 provides the feedback signal to

the operational amplifier 230. In one embodiment, the sensing circuit 235 includes the PMOS transistors Q17 and Q18, biased by the voltage, voh_bias 204. Thus, a feedback path is provided in between the current source Q19, output voltages lvds out_p 291 and lvds out_n 292, and the operational amplifier 230. When lvds out_p 291 is higher than lvds out_n 292, more current flows through the PMOS transistor Q17 than the PMOS transistor Q18. Thus, in this case, the output voltage, voh_sense 208, of the sensing circuit 235 corresponds to lvds out_p 291. Likewise, when lvds out_n 292 is higher than lvds out_p291, more current flows through the PMOS transistor Q18 than the PMOS transistor Q17. Thus, voh_sense 208 corresponds to lvds_n 292 in this case. The operational amplifier 230 may drive the current source Q19 in response to both voh_ref 205 and voh_sense 208 from the sensing circuit 235.

[0020] One should appreciate that the embodiment of the LVDS output driver described above is for illustration, not limitation. Additional circuit components or electronic devices not shown in Figure 2 may be included in some embodiments of the LVDS output driver without departing from the spirit and scope of the appending claims.

[0021] Figure 3 shows one embodiment of a process to output low voltage differential signals. At block 310, a number of input signals are amplified using inverters. At block 320, the amplified input signals are provided to a number of pull-up transistors from the inverters. At block 330, each of the pull-up transistors is coupled to one of a set of pull-down transistors. Each of the pull-down transistors may include a source, a drain, a gate, and a bulk terminal. A pull-up transistor may be coupled to the source of one of the pull-down transistors. At block 340, the bulk terminal of each of the

pull-down transistors is coupled to the source of the corresponding pull-down transistor to reduce body effect on the corresponding pull-down transistor.

[0022] At block 350, a current is supplied to the pull-up transistors from a current source. At block 360, the higher output voltage among the low voltage differential signals is sensed to produce a feedback signal. At block 370, the current source is driven using an operational amplifier in response to the feedback signal.

[0023] At block 380, differential low swing signals are generated using a low swing differential pre-driver. The pull-down transistors are driven with the differential low swing signals in response to the input signals at block 390 to produce low voltage differential signals at the sources of the pull-down transistors.

[0024] Figure 4 shows one embodiment of a process to generate differential low swing signals using a low swing differential pre-driver. At block 410, a current is supplied to a load in a low swing differential pre-driver from a current source. The load may include a resistor having two nodes. At block 420, the current from the load is sunk from the load via a transistor and a resistor. The transistor and the resistor may be coupled to each other in parallel. At block 430, a pair of low swing differential signals are output via the load. In one embodiment, the low swing differential signals are applied to the gates of the pull-down transistors in a LVDS driver to drive the pull-down transistors.

[0025] Figure 5 illustrates an exemplary embodiment of a networked system 500. The system 500 includes a network interface 510 having a LVDS output driver 515, transmission lines 530, and a network component 540. One example of the network component 540 is a storage device, such as a hard drive, a disk, etc. In one embodiment,

the network interface 510 is an Ethernet interface. The network interface 510 is coupled via the LVDS output driver 515 and the transmission lines 530 to the network component 540. Signals may be transmitted between the network interface 510 and the network component 540 via the transmission lines 530. To send signals from the network interface 510 to the network component 540, the network interface 510 uses the LVDS output driver 515 to drive the signals onto the transmission lines 530. Exemplary embodiments of the LVDS output driver 515 have been discussed above with reference to Figure 2.

[0026] Note that any or all of the components of the networked system 500 and associated hardware may be used in various embodiments of the present invention. However, it can be appreciated that other configurations of the networked system may include some or all of the components illustrated in Figure 5. Furthermore, other embodiments of the networked system may include additional components not illustrated in Figure 5.

[0027] The foregoing discussion merely describes some exemplary embodiments of the present invention. One skilled in the art will readily recognize from such discussion, the accompanying drawings, and the claims that various modifications can be made without departing from the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting.